* **Gates**

- 5 x 74 LS/HC 11 Triple 3-input AND gate

- 3 x 74 LS/HC 32 Quad 2-input OR gate

- 1 x 74 LS/HC 74 ON Semiconductor- Dual D Flip-Flop

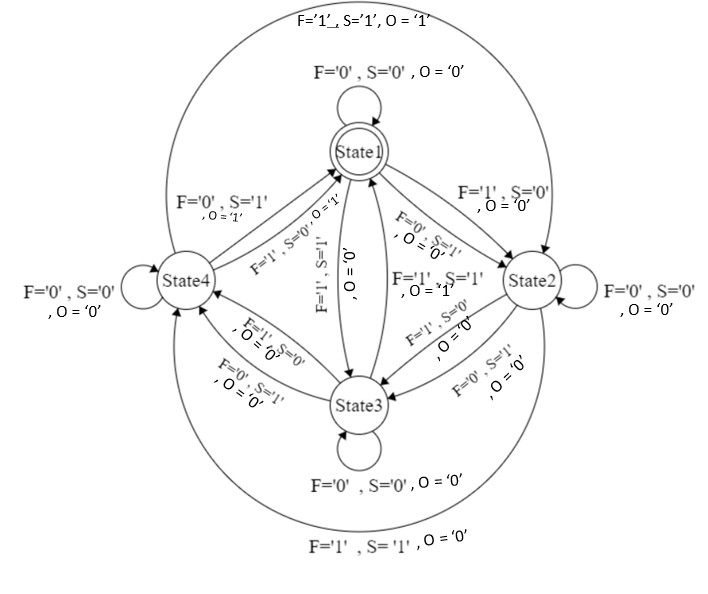
- 1 x 74 LS/HC 163 NXP Semiconductors - Presentable synchronous 4-bit binary counter

* **Objective**

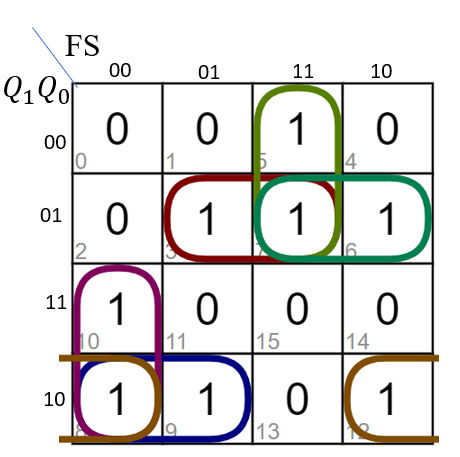
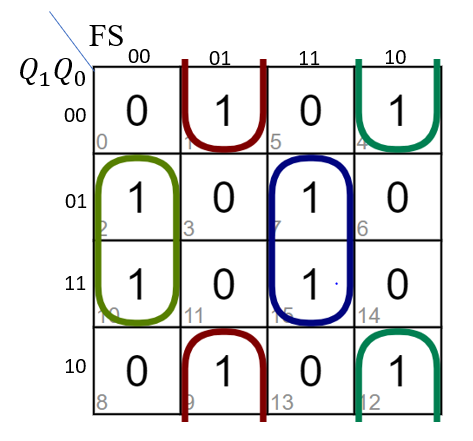
In this week’s lab experiment we are assigned to implement a Finite State Machine with various integrated circuit on the breadboard. I am going to implement a setup, a game of flipping coins, with FSM. Doing so I am going to use AND gates, OR gates, D Flip-Flop and for the input a synchronous 4-bit binary counter for my implementation.

* **Design Specification Plan**
* I am going implement a game, in which player will have two coins and s/he will flip two coins at the same time. If a head of the coin come its worth is ‘1’ point, if tail of the coin comes it is ‘0’ points. The aim of the game is collecting 4 points. Player can earn 0-point, 1-point or max 2-points at an attempt. Number of the attempts are not important, only thing important is collecting 4 points.
* **Proposed Design Methodology**
* I started my design from state diagram, in which I have 4 states. States are state1 is 0-point, state2 is 1-point, state3 is 2-points and last state, state4 is 3-points. F is the first coin and S is the second coin.

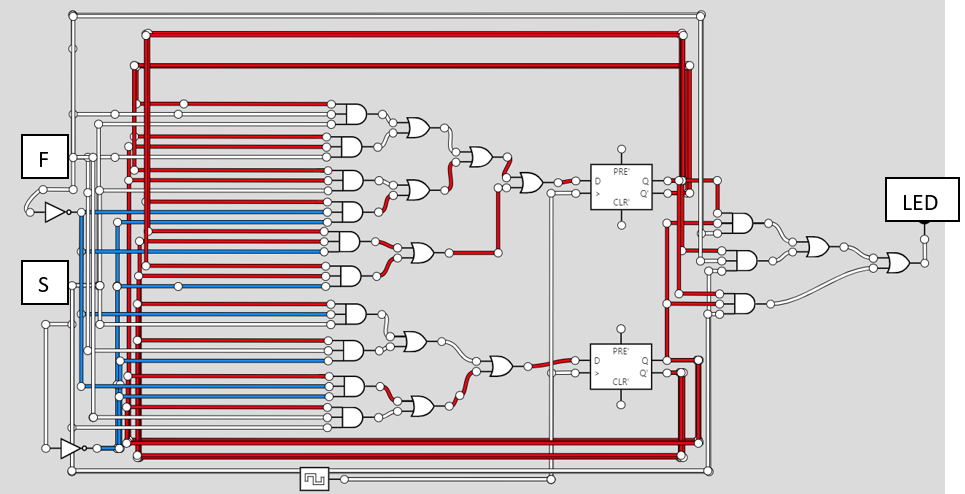
State diagram



* After drawing state diagram, I draw my Karnaugh maps to find and ,the inputs of the D Flip-Flop, which is determined by outputs of the D Flip-Flop and and inputs F and S.

* According to my K- maps I find my SOPs of and .
* Looking for these equations I draw my schematic design of the desired circuit.



* Looking at y schematic I find the IC that I need and how many of them I will in my implementation.

